Remarks/Arguments:

Claims 8 and 12 have been objected to. Claims 8 and 12 have been appropriately amended.

Claims 8 and 12 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Arita (U.S. Patent No. 6,046,467). It is respectfully submitted, however, that the claims are patentable over Arita for the reasons set forth below.

Claim 8 recites "a material for the upper electrode is evaporated on the titanium material layer and lifted off." Owing to this structure, there is no possibility of damaging the titanium material layer under the upper electrode. Thus, a) the film thickness of the titanium material layer under the upper electrode after the lift-off and b) the film thickness of the titanium material layer other than the portion under the upper electrode after the lift-off, become uniform. As such, it is possible to obtain a flat titanium material layer.

As a result, there is no possibility of damaging the titanium material layer near the end portion of the upper electrode after the lift-off or there is no possibility that a difference in the film thickness of the titanium material layer occurs. Thus, it is possible to obtain an excellent semiconductor device with the suppression of leak current.

On the other hand, in Arita, the top electrode 24 is etched by a dry-etching method (col. 3, line 22), thereby damaging the capacitor insulating layer 23 under the top electrode 24 and causing a difference between the film thickness of the titanium material layer under the upper electrode after the lift-off and the film thickness of the titanium material layer other than the portion under the upper

electrode after the lift-off. Thus, it is impossible to obtain a flat capacitor insulating layer 23.

Arita (col. 3, line 22) describes "selectively" etching the top electrode 24 by a dry-etching method. However, even if an etching is performed selectively, damage to the capacitor insulating layer 23 due to a high energy particle cannot be avoided as long as the dry-etching method is used. This damage reduces the film thickness of the capacitor insulating layer 23 and the like, and reduces the crystallinity of the capacitor insulating layer 23.

In Arita, as described above, a difference of the film thickness of the capacitor insulating layer 23 occurs near the end portion of the upper electrode after the lift-off and the crystallinity is decreased, thus resulting in a leak current. As such, it is not possible to obtain an excellent semiconductor device.

For this reason, claim 8 is patentable over Arita.

Claim 12 of the present application depends from claim 8. As such, claim 12 is allowable in view of its dependency on allowable claim 8.

Claim 12 additionally recites "a material for the lower electrode is evaporated on the silicon oxide layer and lifted off."

Owing to this structure, there is no possibility of damaging the silicon oxide layer under the lower electrode. Thus, the film thickness of the silicon oxide layer under the lower electrode after the lift-off and the film thickness of the silicon oxide layer other than the portion under the lower electrode after the lift-off become uniform. As such, it is possible to obtain a flat silicon oxide layer.

Thus, there is no possibility of damaging the silicon oxide layer near the end portion of the lower electrode after the lift-off or there is no possibility that a difference in the film thickness of the silicon oxide layer occurs. Thus, it is possible to obtain an excellent semiconductor device with the suppression of leak current.

On the other hand, in Arita, the bottom electrode 22 is etched by a dry-etching method (col. 3, line 22), thereby damaging the insulating layer 21a under the bottom electrode 22 and causing a difference between "the film thickness of the silicon oxide layer under the lower electrode after the lift-off" and "the film thickness of the silicon oxide layer other then the portion under the lower electrode after the lift-off." Thus, it is impossible to obtain a flat insulating layer 21a.

Arita (col. 3, line 22) describes "selectively" etching the bottom electrode 22 by a dry-etching method. However, even if an etching is performed selectively, damage to the insulating layer 21a due to a high energy particle cannot be avoided as long as the dry-etching method is used. This damage reduces the film thickness of the insulating layer 21a and the like, and reduces the crystallinity of the insulating layer 21a.

In Arita, as described above, a difference of the film thickness of the insulating layer 21a occurs near the end portion of the lower electrode after the lift-off and the crystallinity is decreased, thus resulting in a leak current. As such, it is difficult to obtain an excellent semiconductor device.

In view of the reasons set forth above, the above-identified application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

LEA/fp

Dated: February 27, 2007

P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

February 27, 2007 Fran Petrillo

FP_117231